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Atty. Dkt. No. 039153-0688

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ihsan J. DJOMEHRI

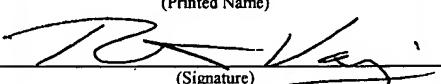
Title: STRAINED SILICON MOSFETS
HAVING NMOS GATES WITH
WORK FUNCTIONS FOR
COMPENSATING NMOS
THRESHOLD VOLTAGE SHIFT

Appl. No.: 10/738,496

Filing Date: 12/17/2003

Examiner: V. Hung

Art Unit: 2811

CERTIFICATE OF EXPRESS MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
EV 420553517 US (Express Mail Label Number)	August 30, 2004 (Date of Deposit)
Ruthie Vallejo (Printed Name)	
 (Signature)	

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the restriction requirement set forth in the Office Action mailed August 13, 2004, Applicant hereby provisionally elects Group II, Claims 9-22, drawn to a method of making a semiconductor device, classified in class 438, subclass 592. Applicant reserves the right to file a divisional application on the non-elected claims.

Respectfully submitted,

Date 30 August 04

By Ronald Coslick

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